

In the Claims:

Please cancel claims 9-13, without prejudice or disclaimer, as indicated in the following listing of claims, which replaces all previous versions.

1. *(Previously Presented)* Method for forming a strained Si layer, comprising:
 formation of an epitaxial SiGe layer on a monocrystalline Si surface layer of a substrate, the substrate including a support layer and a buried silicon dioxide layer, the monocrystalline Si surface layer residing on the buried silicon dioxide layer,
 ion implantation of said Si surface layer and said epitaxial SiGe layer to transform said Si surface layer into an amorphous Si layer and a portion of said epitaxial SiGe layer into an amorphous SiGe layer, a further portion of said epitaxial SiGe layer being a remaining monocrystalline SiGe layer,
 said amorphous Si layer, said amorphous SiGe layer and said remaining monocrystalline SiGe layer forming a layer stack on said buried silicon dioxide layer,
 depositing a silicon dioxide capping layer on said remaining monocrystalline SiGe layer,
 bonding the silicon dioxide capping layer to a silicon dioxide surface layer of a second substrate and thereafter removing said support layer and said buried silicon dioxide layer by etching.
2. *(Previously Presented)* Method according to claim 1, further comprising patterning of said layer stack for forming active parts of a MOSFET structure.
3. *(Cancelled).*
4. *(Previously Presented)* Method according to claim 1, further comprising:
 re-crystallizing of said amorphous Si layer and said amorphous SiGe layer by a solid phase epitaxy regrowth process at an interface between said remaining monocrystalline SiGe layer and said amorphous SiGe layer,

said amorphous Si layer being transformed into an epitaxial strained Si layer and
said amorphous SiGe layer being transformed into a re-grown crystalline SiGe layer.

5. *(Cancelled)*.
6. *(Previously Presented)* Method according to claim 1, characterized in that said strained Si layer is a gate channel in a MOSFET structure.
7. *(Previously Presented)* Method according to claim 4, characterized in that an annealing temperature during said solid phase epitaxy regrowth process is substantially below 600° C.
8. *(Previously Presented)* Method according to claim 1, characterized in that said Si surface layer has a thickness of less than 10 nm.

Claims 9-13 *(Cancelled)*